

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE (REV. 7-80) PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	ATTY. DOCKET NO. 030284	SERIAL NO. Unknown <i>10/644 490</i>
	APPLICANT Amr Fahim	
	FILING DATE August 19, 2003	GROUP Unknown
	DATE MAILED: <u>August 19, 2003</u>	

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	Ref No	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPRO- PRIATE
	A1						
	A2						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	Ref No	DOCUMENT NUMBER	DATE	COUNTRY	NAME	CLASS	SUB CLASS
	B1						
	B2						

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Page, Etc.)

<i>Jv.</i>	C1	Ahn, et al., "A Low-Jitter 1.9-V CMOS PLL for UltraSPARC Microprocessor Applications", IEEE Journal of Solid-State Circuits, Vol. 35, No. 3 March 2000 pps. 450 - 454
<i>Jv.</i>	C2	John Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11 November 1996, pps. 1723-1732
<i>Jv.</i>	C3	Wu, et al., "A Low Glitch 10-bit 75 MHz CMOS Video D/A Converter", IEEE Journal of Solid-State Circuits, Vol. 30, No. 1, January 1995, pps. 68 - 72.
<i>Jv.</i>	C4	Chung, et al., "An All-Digital Phase-Locked Loop for High-Speed Clock Generation", IEEE Journal of Solid-State Circuits, Vol. 38, No. 2, February 2003, pps. 347 - 351
<i>Jv.</i>	C5	Hwang, et al., "A Digitally Controlled Phase-Locked Loop with a Digital Phase-Frequency Detector for Fast Acquisition," IEEE Journal of Solid-State Circuits, Vol. 36, No. 10, October 2001, pps. 1574 - 1581
EXAMINER <i>Jv.</i>		DATE CONSIDERED <i>4/26/05</i>

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Sheet 1 of 1

FORM PTO-1449 (REV. 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 030284	SERIAL NO. 10/644.490
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use several sheets if necessary)</i>		APPLICANT Amr Fahim	
		FILING DATE 08/19/2003	GROUP UNKNOWN
		DATE MAILED: 03/17/05	

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
Dr.	A1 6 0 5 4 9 0 3	04/25/00	Fiedler	331	17	
Dr.	A2 6 6 0 6 3 6 4	08/12/03	Walley et al.	375	376	
	A3					
	A4					
	A5					
	A6					

U.S. PATENT APPLICATION PUBLICATION DOCUMENTS

*EXAMINER INITIAL	PUBLICATION NUMBER	PUB. DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
Dr.	B1 2 0 0 1 0 0 3 3 2 0 0 A1	10/25/01	Staszewski et al.	331	18	
	B2					

EXAMINER INITIAL	Ref No	DOCUMENT NUMBER	DATE	COUNTRY	NAME	CLASS	SUB CLASS
	C1						
	C2						
	C3						
	C4						
	C5						

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Page, Etc.)

	D1	
	D2	
EXAMINER	<i>Amr</i>	
DATE CONSIDERED	4/26/05	
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